IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Amended): A semiconductor device manufacturing method of forming a second conductivity-type region by irradiating impurity ions onto a first conductivity-type semiconductor substrate;

wherein the irradiating impurity ions is performed to form a junction structure comprising a vertical junction group where a first conductivity-type region and the second conductivity-type region are alternatively arranged vertically to a surface of the semiconductor substrate; and

wherein the impurity ion irradiated region is restricted by a shield mask intercepting said impurity ions and the impurity ion acceleration energy is controlled to provide a uniform impurity distribution in the direction of irradiation in said second conductivity-type region.

Claim 2 (Twice Amended): A semiconductor device manufacturing method of forming at least one of a first and second conductivity-type regions in a semiconductor substrate by selectively irradiating impurity ions onto said semiconductor substrate;

wherein the selectively irradiating impurity ions is performed to form a junction structure comprising a vertical junction group where the first conductivity-type region and the second conductivity-type region are alternatively arranged vertically to a surface of the semiconductor substrate; and

wherein the impurity distributions in said first and second conductivity-type regions are uniform in the direction of irradiation, and the impurity ion acceleration energy and the area of each region irradiated by said impurity ions are controlled so that the cross-sectional shape and cross-section area of said first and second conductivity-type regions on planes

perpendicular to the direction of irradiation [may be] are uniform in the direction of irradiation.

Claim 3 (Original): The semiconductor device manufacturing method according to claim 2, wherein the control of the area of said irradiated region comprises the steps of forming an ion beam made of impurity ions and sweeping the ion beam in the vertical and horizontal directions on the irradiated region, and the acceleration energy and the area of the irradiated region are controlled by changing the area of said irradiated region according to changes in said acceleration energy.

Claim 4 (Original): The semiconductor device manufacturing method according to claim 3, wherein said impurity ion beam is electrically swept on the irradiated region.

Claim 5 (Original): The semiconductor device manufacturing method according to claim 3, wherein said impurity ion beam is magnetically swept on the irradiated region.

Claim 6 (Original): The semiconductor device manufacturing method according to claim 3, wherein said impurity ion beam is swept on the irradiated region by moving the semiconductor substrate.

Claim 7 (Original): The semiconductor device manufacturing method according to claim 3, wherein the acceleration energy and the area of the irradiated region are controlled by decreasing the area of the irradiated region according to increase in the acceleration energy.

Claim 8 (Original): The semiconductor device manufacturing method according to claim 3, wherein the acceleration energy and the area of the irradiated region are controlled by increasing the area of the irradiated region according to decrease in the acceleration energy.

Claim 9 (Original): The semiconductor device manufacturing method according to claim 2, wherein the area of the irradiated region is restricted by a shield mask intercepting said impurity ions, and the acceleration energy and the area of the irradiated region are controlled by changing the area of each opening of said shield mask intercepting impurity ions according to changes in the acceleration energy.

Claim 10 (Original): The semiconductor device manufacturing method according to claim 9, wherein the acceleration energy and the area of the irradiated region are controlled by decreasing the area of each opening of said shield mask intercepting impurity ions according to increase in the acceleration energy.

Claim 11 (Original): The semiconductor device manufacturing method according to claim 9, wherein the acceleration energy and the area of the irradiated region are controlled by increasing the area of each opening of said shield mask intercepting impurity ions according to decrease in the acceleration energy.

Claim 12 (Twice Amended): A semiconductor device manufacturing method of forming a first conductivity-type region and a second conductivity-type region on a semiconductor substrate by irradiating impurity ions onto said semiconductor substrate;

wherein the irradiating impurity ions is performed to form a junction structure comprising a vertical junction group where the first conductivity-type region and the second conductivity-type region are alternatively arranged vertically to a surface of the semiconductor substrate; and

wherein the regions irradiated by impurity ions are restricted by impurity ion intercepting shield masks which are in an inverted imaging relation to each other so that the cross-sectional shape and the cross-section area of the first and second conductivity-type regions on planes perpendicular to the direction of irradiation [may be] are uniform along the direction of irradiation, and the impurity ion acceleration energy is controlled to make the impurity ion distributions in the first and second conductivity-type regions uniform along the direction of irradiation.

Claim 13 (Original): The semiconductor device manufacturing method according to claim 12, wherein said impurity ion intercepting shield masks which are in an inverted imaging relation to each other are formed by printing the same mask patterns on the semiconductor substrate by the use of a positive resist and a negative resist.

Claim 14 (Original): A semiconductor device manufacturing method of forming an N^+ region by irradiating a neutron beam onto a semiconductor ingot having a P^+ region;

wherein the incident direction of said neutron beam is collimated to make the cross-sectional shape and the cross-section area of said N^+ region on planes perpendicular to the direction of irradiation uniform along the direction of irradiation, and the impurity distribution in said N^+ region is controlled to be uniform along the direction of irradiation.

Claim 15 (Original): The semiconductor device manufacturing method according to claim 14, wherein the semiconductor having the P^+ region is an P^+ type semiconductor ingot and the incident direction of said neutron beam is parallel to the growth axis of said P^+ type semiconductor ingot.

Claim 16 (Original): The semiconductor device manufacturing method according to claim 14, wherein said semiconductor ingot is made of silicon.

Claim 17 (Original): The semiconductor device manufacturing method according to claim 14, wherein said semiconductor ingot is made of germanium.

Claim 18 (Original): The semiconductor device manufacturing method according to claim 14, wherein said semiconductor ingot is made of silicon carbide.

Claims 19-32 (Canceled).

Claim 33 (New): The semiconductor device manufacturing method according to claim 1, wherein the first conductivity-type region includes plural portions, the second conductivity-type region includes plural portions, and the plural portions of the first conductivity-type region are alternatively arranged with the plural portions of the second conductivity-type region and vertically to the surface of the semiconductor substrate.

Claim 34 (Canceled).

Claim 35 (New): The semiconductor device manufacturing method according to claim 2, wherein the first conductivity-type region includes plural portions, the second conductivity-type region includes plural portions, and the plural portions of the first conductivity-type region are alternatively arranged with the plural portions of the second conductivity-type region and vertically to the surface of the semiconductor substrate.

Claim 36 (Canceled).

Claim 37 (New): The semiconductor device manufacturing method according to claim 12, wherein the first conductivity-type region includes plural portions, the second conductivity-type region includes plural portions, and the plural portions of the first conductivity-type region are alternatively arranged with the plural portions of the second conductivity-type region and vertically to the surface of the semiconductor substrate.